Prof Name: TG Venkatesh, IITM

Relevant Course: Digital Electronics

Topic Name: Digital System Design

Relevant Department: Electrical and Computer Science

Relevant Semester: 3rd Semester students onwards

Pre- requisites: Nil

Preferred Date and Time for Session: 6th Feb, 13th Feb and 17th Feb (10-12pm)

OUTLINE

SEQUENTIAL CIRCUITS

Flip-flops: SR, D, T, JK. Meta stability of flip-flops, **Registers**: shift registers, **Counters**: synchronous and asynchronous, Binary counter, Modulo Up and down counter, **Synchronous Counter design** using flip-flops, VHDL models for flip-flops, **Memory devices**: ROM

FINITE STATE MACHINES

Mealy and Moore machines: sequence detector, Mealy and Moore machine comparison, **Sequential network design**: state table, state graph. **State table reduction** using row reduction, using implication tables. State assignment rules, Equivalent state machines.

ASM (ALGORITHMIC STATE MACHINE) CHARTS

State machine design using SM charts, ASM realization using traditional method, MUX based design, one hot method, ROM based method.

Design Examples: Traffic light controller, Dice game. Basics of asynchronous sequential networks